Advancements in indirect Time of Flight image sensors in front side illuminated CMOS

Markus Dielacher
Infineon Technologies
Graz, Austria
markus.dielacher@infineon.com

Martin Flatscher
Infineon Technologies
Graz, Austria
martin.flatscher@infineon.com

Reinhard Gabl
Infineon Technologies
Graz, Austria
reinhard.gabl@infineon.com

Richard Gaggl
Infineon Technologies
Villach, Austria
richard.gaggl@infineon.com

Dirk Offenberg
Infineon Technologies
Dresden, Germany
dirk.offenberg@infineon.com

Jens Prima
pmdtechnologies ag
Siegen, Germany
j.prima@pmdtec.com

***Abstract*— We will present major advances in Time of Flight (ToF) image sensors for consumer applications. Several innovative elements integrated into a 130nm front side illumination CMOS node reveal superior sensor performance so far only attributed to much more complex backside illumination technologies. The gate controlled pixels comprising deep trenches, buried mirrors and integrated prisms, reveal high quantum efficiency and modulation transfer function (MTF) close to the physical pixel size. In-pixel common mode suppression prevents saturation even under backlight conditions. The comprehensive System on Chip integrates high speed ADCs, a flexible phase shifter, as well as current monitoring for laser safety.**

Keywords—iToF, Pixel, Buried Mirror

I. Introduction

Different active and passive 3D imaging systems have already been developed to penetrate the consumer market. They are based either on 3D triangulation supported by RGB stereo cameras combined with feature-extraction algorithms or they follow an active approach such as structured light or ToF. Smartphone applications such as front camera supporting face recognition, or rear camera enabling virtual- or augmented reality, operate at moderate distances of up to 5 meters and require accurate measurements of about 1 to 5 mm. For this kind of application, time-of-flight imaging is a competitive technology. In this case, the time it takes for light emitted from the device to reflect off objects in the scene and return to the sensor is measured.

This work is focusing on indirect ToF (iToF) where the time of flight is not measured directly in the time domain, but in the phase domain. The main advantage of this approach compared to direct ToF (dToF) is that not each pixel requires its own time to digital converter (TDC) but the readout circuits can be shared, thus the pixel pitch can be smaller and the number of pixels can be higher.

The employed CMOS and pixel technology will be discussed in the next section showing the improvement of Quantum Efficiency (QE). A novel pixel development will be presented in section III introducing a photonic mixing device (PMD) with Suppression of Background Illumination (SBI). The key performance parameters such as demodulation contrast and Modulation Transfer Function (MTF) will be discussed as well. Section IV shows the SoC implementation of the whole CMOS Imager System (CIS) focusing on the readout path, Laser safety and the generation of all required phases for the PMD. Measurement results and a comparison with state of the art CIS will conclude this paper, showing that the improved FSI process can compete with more expensive BSI technologies.

II. CMOS Technology

As technology platform, Infineon's robust and automotive qualified 0.13µm node is used demonstrating proper performance with comprehensive libraries. It is an excellent base technology for monolithic integration of a front side illuminated (FSI) PMD. The PMD is arranged side by side to CMOS to enable low costs compared to two wafer solutions requiring stacking and backside illumination (BSI). An improved set of design rules is used to enable smaller pixel pitches. A set of new 1V5 analog transistors is developed with 2.2nm gate oxide (GOX) thickness combined with shallow pixel specific wells allowing shrinkage of read out circuit thus good performance and transistor matching. A 45° rotation of transistors is allowed to enable different pixel geometries and flexible arrangement of the pixel read out circuit and the photosensitive areas within the pixel array.

Three additional optical elements were developed to enhance the performance (see Fig. 1):

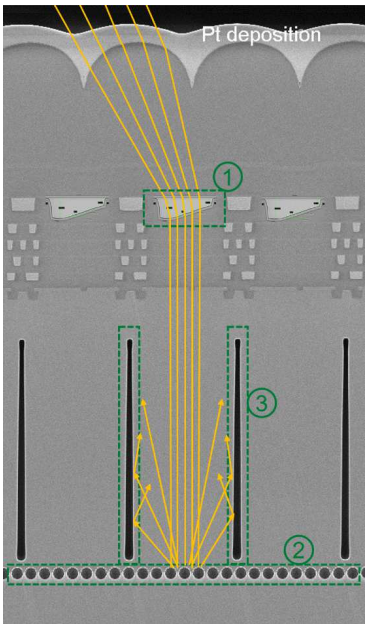

Fig. 1. Pixel cross section showing (1) prism, (2) mirror, and (3) deep trench

1.) Prism: An individual prism for each pixel is implemented to correct the chief ray angle (CRA) of the

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incident light especially at the edge of the pixel array. Chief ray angles up to 45° can be compensated. Amorphous silicon has been chosen as prism material due to high refractive index and good transparency at 940nm wavelength. Combined with µlenses, the limitations in pixel pitch by metal stack are overcome and crosstalk is reduced even with Epi film thicknesses above 10µm. All pixels exhibit perpendicularly illuminated behavior.

2.) Mirror: Underneath the photosensitive region a buried mirror is installed to increase the QE. The mirror can be realized either as a cavity with planar surface or as an array of separated cavity spheres to include a scattering effect. Reflectivity of 75% is reached. To eliminate dark current a barrier implant layer is used between mirror and sensitive region.

3.) Deep Trench: To prevent optical and electrical x-talk and enable small effective pixel pitches a deep trench isolation (DTI) is implemented. These DTI allow a photosensitive depth above 10µm in combination with outstanding crosstalk performance. The trench surface is passivated to suppress dark current generation. The deep trench is buried, therefore not consuming any area of silicon surface and enabling maximum degrees of freedom for circuitry. The high quality silicon above the deep trenches allows transistor devices directly on top of trenches without any concern to GOX integrity or other reliability or performance relevant topics.

The additional optical elements can be modularly implemented depending on pixel pitch and requirements of the product.

III. Pixel Development

Several pixels with 10µm, 7µm and 5µm pixel pitch have been realized in the technology described above. We will focus on the more challenging 7µm and 5µm pixel pitches in the following section.

Fig. 2 depicts the schematic of the 7µm pixel exemplarily. The core device of the 7µm and 5µm pixels is based on a photonic mixing device. This PMD consists of two photogates (PG A/B), which are each connected to an integrating diode (ID A/B). Each tap is then connected to its readout circuit (RO), consisting of a reset (RES) and hold (H) switch as well as a source follower transistor (SF) and a select (SEL) switch.

An additional circuit (SBI), consisting of 5 transistors designed as a current mirror, is integrated within each pixel. This SBI is arranged between the two RO channels and guarantees the suppression of photocurrent, generated by background illumination (i.e. sunlight). Fig. 3 shows the working principle of this SBI. Fig. 4 illustrates the expansion of the pixel operating range beyond 30klux background illumination using this SBI. Fig. 5 illustrates the aggressive electronic layout approach, which is required to integrate the five additional transistors of the SBI circuit into the pixel. In this architecture the photosensitive PMD areas and non-photosensitive pixel circuitry (SF, SEL, SBI, RES, H) areas are alternating like a checkerboard pattern to get a high fill factor and a symmetrical layout. The microlenses are centered on the photosensitive area correspondingly.

An additional technology option permits the rotation of this architecture by 45°. A special set of 1V5 transistors with thin gate oxide has been developed for the 5µm pixel. These 1V5 transistors fulfill the matching requirements of the SBI current source transistors in channel A/B in combination with the small transistor dimension requirements. The 1V5 thin GOX transistors have been process-adapted to the 45° rotation to ensure their electrical behavior. The voltage operating range of these 1V5 transistors has been adapted by a virtual pixel ground connection to 1.8V.

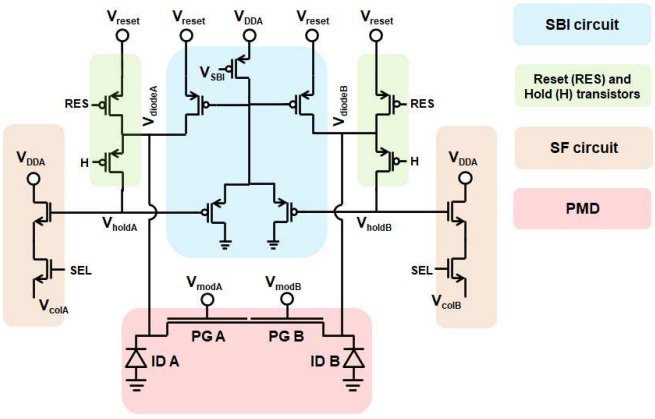

Fig. 2. Pixel schematic for 7µm pixel

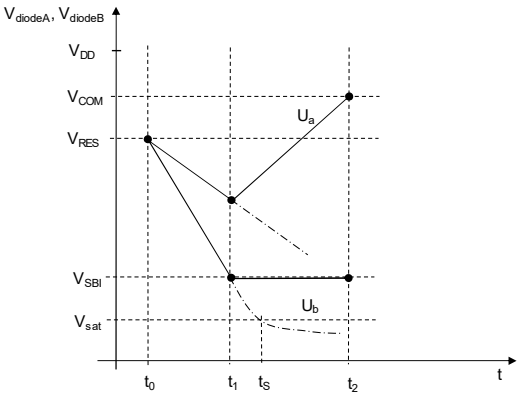

Fig. 3. Working princple SBI: channel B with higher signal from photocurrent reaches V_{SBI} threshold first. Saturation is avoided by a compensation current in channel A and B.

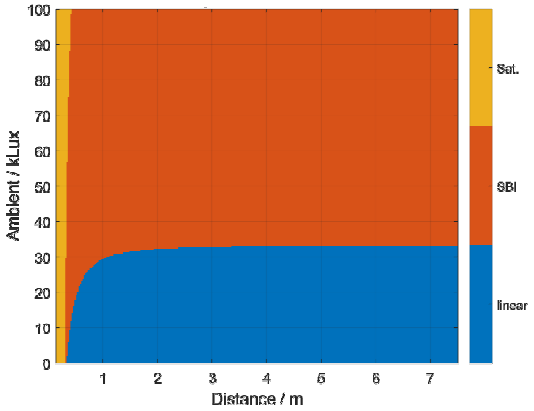

Fig. 4. Expansion of pixel operating range in background light with SBI (simulated: 1W 940nm VCSEL, 50nm optical filter, F# 1.58, 500µs T_{int}, 90% target reflectivity)

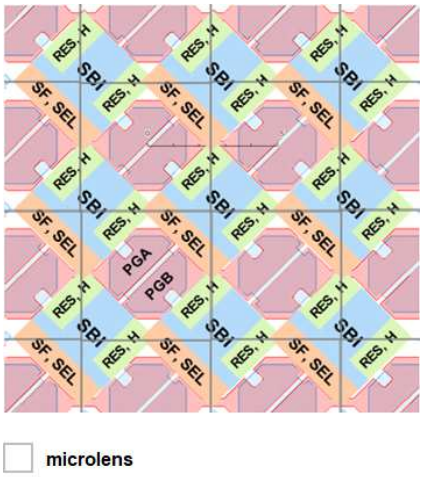

Fig. 5. Layout of rotated 5µm pixel

IV. SENSOR ARCHITECTURE

Development of new pixel generations is supported by a flexible product architecture, shown in Fig. 6, which can be adapted to different pixel sizes and resolutions and has already been proven in different products available on the market. It is based on a programmable microcontroller which connects and controls all analog and digital units.

Readout of the pixels is performed with a bank of successive approximation register (SAR) ADCs. Each of the ADCs comes with two input stages which are controlled in ping-pong operation. While an ADC is converting the differential voltage between the first pair of sampling capacitors into a 12 bit output value, the second pair of capacitors is already sampling another pixel and vice versa. Each of the ADCs achieves a sample rate of 7.5 MS/s. The number of instantiated ADCs can be chosen to achieve a certain overall data rate and readout time. As an example, the conversion of 150k pixels within 1.3ms, requires a bank of 16 ADCs. Also the number of DPHY lanes for the transmission of the data to the host processor can be selected such that it fits to the overall data rate.

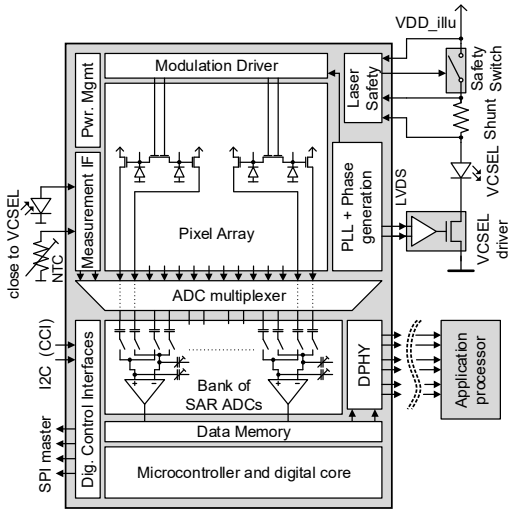

Fig. 6. Top level sensor architecture

Beside the pixel readout, the same ADCs are also used during production test and to convert other internal and external signals via a measurement interface. These signals can include external temperature sensors, photodiodes, or capacitive / resistive coatings to monitor the integrity of the diffuser.

To support laser safety, the sensor provides a dedicated current monitor which continuously monitors the current through the light source and controls a safety switch which disables the light source in case of an overcurrent. To guarantee safety also in case of a defect this current monitor is totally independent from the rest of the system. It includes a dedicated oscillator, separate power domain and independent state machine.

The phase generation shown in Fig. 7 unit cannot only apply defined phase shifts to the modulated illumination signal, but it also supports more complex modulation schemes in order to reduce or remove systematic errors, to increase robustness against interfering signals or to resolve range ambiguities as proposed in [1].

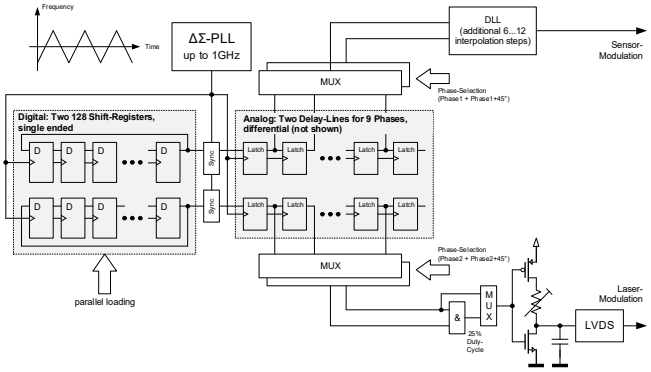

Fig. 7. Detailed architecture of phase generation unit

The modulation waveform is based on two 128bit codes, stored in shift registers. These codes are shifted through analog delay lines based on a modulation clock generated by a ΔΣ PLL. PLL frequency can be up to 1GHz in order to enable oversampling of the codes. Additionally the clock is frequency modulated to support handling of Multi-ToF-Camera scenarios. The analog delay lines are designed in a fully differential manner (not shown in the picture) and make use of both clock edges. One out of nine output phases can be selected with a multiplexer for the illumination and for the sensor path independently. With help of a delay-locked loop (DLL) the phase resolution is additionally improved. In the illumination path, the duty cycle of the signal can be adjusted in three different ways: (1) with a modulation code, (2) by combining two phases of the analog delay line, or (3) with help of an analog programmable delay. A fine adjustment of the duty-cycle is required to maximize the ratio of the fundamental in the emitted light and illumination current consumption. A low duty cycle also optimizes the pixel contrast as shown in Fig. 9.

An example: A 100MHz modulation frequency can be generated with an oversampling rate of 10. This allows to program phases in steps of 36°. With help of the analog delay line, finer steps can be programmed (in 18° steps). By using the DLL, these steps can be divided into six 3° phases. The fine resolution is needed to support camera calibration.

V. Measurement Results

Fig. 8 shows a micrograph of a chip including a sensor core with 153k pixels of 7µm pitch, an array of 16 ADCs and a DPHY interface with two data lanes.

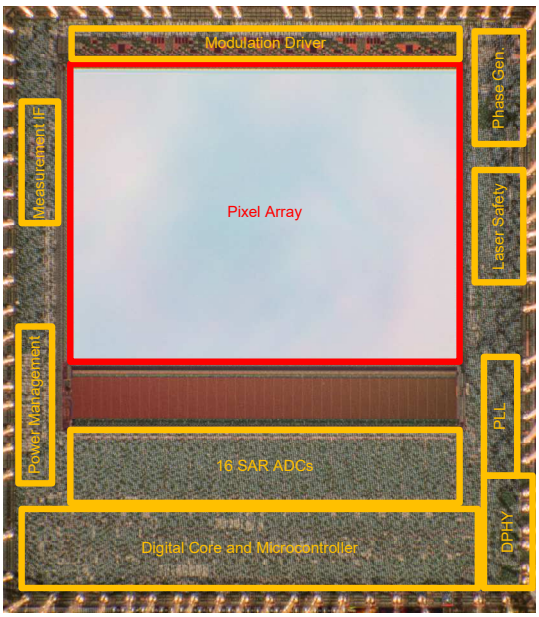

Fig. 8. Chip Micrograph of sensor with 153k 7µm pixels

Table 1 summarizes some key parameters of the developed sensors. Due to the mirror and the resulting longer effective light-path through the pixel, the quantum efficiency of the 5µm and 7µm could be increased up to 28% and 32%, respectively.

Table 1: Performance summary and comparison

	this work	**this work**	**[2]**	**[3]**	**[4]**	**[5]**	**[6]**
Process node	130nm fsi	130nm fsi	65nm stacked BSI	65nm BSI	65nm BSI	90 nm / 65nm stacked BSI	65nm BSI
pixel pitch	5 µm	7 µm	3.5 µm	7 µm	3.5 µm	3.5 µm	2.8 µm
#pixels	307k	153k	1.2M	307k	1M	1.2M	1.2M
QE @ 940 nm	28%	32%	38%	34%	44% @860 nm	32%	36%
Contrast @ 100 MHz	86%	91%	96%	86%	87% @200 MHz	95%	86%

High contrast values of 86% and 91% at 100MHz for the 5µm and 7µm pixel could be achieved by careful harmonization of DTI passivation and the doping of the epitaxial layer. Fig. 9 illustrates the contrast behavior for different duty cycles (DC) and modulation frequencies, normalized to the contrast for short DC at 80MHz. As can be observed, the contrast can be increased by decreasing the DC. In most applications the image sensor chip is usually operated at a DC of 30%.

The impact of crosstalk on the spatial resolution of the imager can be expressed by means of an effective pixel pitch. To determine this effective pitch, we first calculate the MTF by measuring the point spread function of an illuminated pixel and taking its Fourier transform. An ideal pixel without crosstalk is then adjusted in pitch until its MTF value at 50% corresponds to the measured MTF at 50%. This adjusted pitch is the effective pitch of the pixel including crosstalk effects. For 5µm pixel pitch with 12µm depth of the photosensitive region an effective pixel pitch of 5.2µm is reached instead of 6.7µm without DTI.

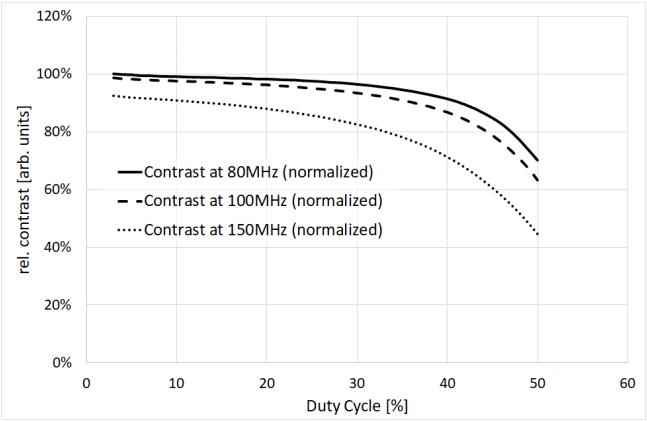

Fig. 9. Rel. contrast vs Duty Cycle for several modulation frequencies. Reduction of Duty Cycle permits higher contrast

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