A 239-298 GHz Power Amplifier in an Advanced 130 nm SiGe BiCMOS Technology for Communications Applications

Thomas Bücher*, Janusz Grzyb*, Philipp Hillger†, Member, IEEE, Holger Rücker†, Bernd Heinemann† and Ullrich R. Pfeiffer*, Fellow, IEEE

*IHCT, University of Wuppertal, 42119 Wuppertal, Germany
†IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Abstract—A broadband 3-stage pseudo-differential SiGe power amplifier, fabricated in an experimental 130 nm SiGe BiCMOS technology with $f_{\text{max}} / f_{\text{sat}}$ of 470/650 GHz, is presented in this paper. Coupled-line matching networks with optimized impedance ratios are used to maximize bandwidth and output power while maintaining flat power gain and group delay for wireless communications applications. The amplifier provides a maximum small-signal power gain of 17.9 dB and a peak $P_{\text{out}}/OP_{\text{dB}}$ of 6.7/5.2 dBM, respectively. A record small-signal and saturated power 3-dB bandwidth of 59 GHz (239-298 GHz) and 89 GHz (226-315 GHz), respectively is achieved. The DC power consumption is about 417 mW with a power-added-efficiency of 0.92% at 267 GHz.

Without the included Balun which is needed for probing, the amplifier’s $P_{\text{out}}$ is increased to 8.1 dBM, while a maximum small-signal gain of 20.2 dB is reached.

Index Terms—SiGe HBT, PA, 6G, Communications, sub-mmWave, Terahertz

I. INTRODUCTION

Recent discussions on demands for 6G hardware have outlined that silicon-based THz systems, e.g. systems addressing the new IEEE 802.15.3d-2017 standard [1], will play a key role for meeting the 100+ Gb/s data rate needs in the future wireless ecosystem [2]. Next-generation high-speed SiGe-HBT technology with $f_{\text{max}} > 600$ GHz [3] promises to allow fundamental device operation in the whole J-band. First works on fully-integrated SiGe-HBT communication links at 240 GHz have demonstrated around 100 Gb/s for 1 m distance [4]. However, supplying high transmission bandwidth (BW) and output power with silicon-based power amplifiers (PA) at around 300 GHz constitutes a significant challenge which will have to be addressed by further technology improvement and design innovation for THz communication. In particular, placing carriers at the boundary of where practical amplification is feasible (approx $f_{\text{max}} / 2$) results in drastically reduced PA capability leading to low gain per stage, low efficiency and, in general, on-the-edge designs with little room for balancing design trade-offs. Moreover, metrics such as gain flatness and group delay variations increase in importance [5] while design methodology is complicated by non-negligible electrical size of transistor cells and via stacks.

The presented power amplifier utilizes an advanced 130 nm SiGe BiCMOS technology which allows reliable amplification above 300 GHz while also generating sufficient output power to e.g. drive frequency-conversion mixers. For input, output and interstage matching, different coupled line structures are used to achieve the high impedance transformation ratios and the compensation of the PA-core capacitances while minimizing losses and maximizing BW (Fig. 1).

Fig. 1. Simplified schematic of the power amplifier. Each amplifier unit cell $(P_{\text{A}_{1,2,3}})$ consists of an EM-optimized cascode layout with optimized current return paths and bypass capacitors. The given input $(Y_{\text{in}})$ and output $(Y_{\text{out}})$ admittances were extracted at 300 GHz, indicating the different Q-factors at input and output. At the input and output of each stage coupled-line matching networks are used for broadband matching.

II. TECHNOLOGY

The circuits are implemented in a development variant of the SiGe BiCMOS technology SG13G3 of IHP. Main features of the HBT technology are outlined in [3]. The high-speed HBTs are integrated in a 130 nm CMOS technology with seven layer aluminum metallization including two thick top metal layers with 2 µm and 3 µm thickness, respectively. The HBT models used for the current designs were extracted from HBTs with peak $f_1$ values of 470 GHz and peak $f_{\text{max}}$ values of 610 GHz corresponding to an early development stage of the BiCMOS process [6]. The HBTs of the present fabrication feature same $f_1$ values and slightly higher $f_{\text{max}}$ values of about 650 GHz as extrapolated from the unilateral power gain at frequencies.
around 20 GHz with an ideal slope of -20 dB/decade. The used HICUM compact transistor models are based on S-parameter measurements up to 67 GHz. Sufficiently accurate S-parameter measurements for the higher frequency bands were not available for the model development.

III. Circuit design

In the presented power amplifier, pseudo-differential cascodes employing transistors with an emitter size of $6 \times (0.96 \times 0.12) \ \mu m^2$ were used. Here, the cascode topology increases the available gain and isolation in addition to the increased voltage swing headroom for maximum output power. The relatively large device size was chosen for higher output currents which again benefits the maximum generated output power. However, the large device size also lowers the cascode’s input and output impedance while increasing the parasitics [7]. The chosen size presents the compromise of high output power generation while still allowing matching to the input and output of the cascode.

The layout of the cascode has additional importance as it creates another limitation to the device size, due to the excess capacitance created by the via stack at the collector node which adds to the device’s internal capacitance. This further increases the Q-factor of the cascode output, and therefore, strongly challenges the design of a broadband matching network at 300 GHz with an additional impedance transformation ratio between different stages. At the same time, the transistor core layout needs to ensure unconditional stability both for differential and common-mode signaling. The AC grounding of the base in the common-base (CB) pair is critical, as it can not only boost the small-signal gain, but can cause oscillation when it is not considered. The same issues arise when modeling the internal nodes between the common-emitter (CE) and CB stages featuring a rather complicated ground-return current flow, which is different for both operation modes. Both of these design concerns increase with device size, creating differences in the electrical lengths connecting different device parts. For this, an optimized electromagnetic layout for the cascode was developed including additional ground paths between the individual devices in a pseudo-differential configuration. Additionally, a distributed-type Metal-Insulator-Metal (MIM) capacitor was added at the CB base node with multi-point contacts to the cascode-stage layout.

For broadband amplifier operation, the impedance transformation potentially provided by the transformer-like matching stages is preferred over the classical matching stub approach. The main purpose of using the transforming sections is the maximization of the voltage swings at the CB output nodes in the presence of a low-impedance termination related to the consecutive stage’s input or the amplifier’s external node. Due to the high Q-factor at the cascode output in conjunction with the required high-impedance transformation ratio, broadband amplifier design at 300 GHz with minimum interstage frequency staggering becomes challenging. Strong interstage staggering may even be detrimental for group-delay distortions which is essential for broadband operation with digitally-modulated waveforms.

Broadband input matching of the power amplifier is relatively easy due to the low Q-factor at the base input of the CE stage. As classical transformers are not feasible at 300 GHz, a set of in-house designed coupled-line distributed transformers were developed. Here, broadside coupling between two buried asymmetric strips with a global close-proximity side ground plane was applied to optimize the transformer layout in the presence of a capacitive-like device-level termination for its broadband operation. The transformers exploit the available 7-layer back end of line (BEOL) stack to widely vary the requested impedance transformation ratio. A non-uniform impedance tapering along the coupled-line sections is further applied for bandwidth optimization. Additionally, the common-mode trap with a broadband device biasing network is provided with an MIM capacitor located centrally in the transformer layout.

To facilitate broadband measurements of the power amplifier for both small- and large-signal operation modes with minimum deembedding effort, a broadband Marchand-type balun with inherent compensation of the on-chip pad low-pass characteristic was placed at the input and output ports of the amplifier. The balun converts the 50 Ω pad-loaded input reference impedance to a differential 100 Ω by means of a coupled-line section with nonuniform characteristic impedance profile. The balun was measured in a back-to-back configuration for the consecutive 2nd-tier deembedding procedure with a maximum insertion loss of 1.5 dB in the entire 220-320 GHz band. The layout was further optimized for common-mode suppression by built-in layout asymmetry, while a ground-patterning was added to prevent the propagation of the common-mode into the substrate.

IV. Measurements

![Fig. 2. Die micrograph of the PA; the bottom Pads are used for DC biasing where each current mirror can be addressed individually. The size of the amplifier excluding the identical signal pads and baluns at the input and output is 380 μm ×180 μm.](Image)

The amplifier, as shown in the micrograph (Fig. 2) was characterized on wafer. The total chip area for this circuit is 0.26 mm², while the amplifier, excluding the baluns and signal pads, covers an area of 0.07 mm². For the small-signal measurements, a Keysight VNA in combination with...
two OML WR3 frequency extenders was used. Here, the TRL calibration was performed on a calibration substrate.

The measured S-parameters of the amplifier can be observed in Figure 3 without further deembedding as the balun does not majorly influence the amplifier performance. The measured parameters show good model-to-hardware correlation. The maximum $S_{21}$ of 17.9 dB is achieved at around 267 GHz, while a total small-signal 3-dB bandwidth of 59 GHz is achieved, from 239 to 298 GHz. The $S_{11}$ and $S_{22}$ values show that the input and output including the baluns are well matched to the probe over a wide frequency range, while displaying minor frequency shifts towards higher frequencies. For high frequencies above 290 GHz, the gain decreases faster than simulated. This is probably due to more rapid gain roll-off as compared to the models derived from extrapolation.

The broadband balun at the input and output allows to observe the amplifier’s frequency behaviour without further need for deembedding. The measured k-factor also shows that the amplifier remains unconditionally stable in the measured frequency range. For communication systems, the group delay introduced by an amplifier is of interest. The symbol duration time for a bit rate of 100 GB/s in a 16-QAM modulation is about 40 ps. The measured PA group delay variation is about ±3 ps in the entire frequency band. Therefore the group delay variation is smaller than 10% of the symbol duration time, showing that the amplifier will not cause noticeable inter-symbol interference in communication systems.

The measured k-factor also shows that the amplifier remains unconditionally stable in the measured frequency range. The measured k-factor is greater than 10 in the entire frequency range. The measured $S_{21}$ is about 17.9 dB at 267 GHz, while a total small-signal 3-dB bandwidth of 59 GHz is achieved, from 239 to 298 GHz. The $S_{11}$ and $S_{22}$ values show that the input and output including the baluns are well matched to the probe over a wide frequency range, while displaying minor frequency shifts towards higher frequencies. For high frequencies above 290 GHz, the gain decreases faster than simulated. This is probably due to more rapid gain roll-off as compared to the models derived from extrapolation.

The measured k-factor also shows that the amplifier remains unconditionally stable in the measured frequency range. For communication systems, the group delay introduced by an amplifier is of interest. The symbol duration time for a bit rate of 100 GB/s in a 16-QAM modulation is about 40 ps. The measured PA group delay variation is about ±3 ps in the entire frequency band. Therefore the group delay variation is smaller than 10% of the symbol duration time, showing that the amplifier will not cause noticeable inter-symbol interference in communication systems.

Fig. 3. Measured and simulated small-signal S-parameters of the presented PA including the balun and pad. The curves show good alignment up to 290 GHz. The stability factor k is greater than 10 in the entire frequency range. The broadband balun at the input and output allows to observe the amplifier’s frequency behaviour without further need for deembedding.

The measured k-factor also shows that the amplifier remains unconditionally stable in the measured frequency range. For communication systems, the group delay introduced by an amplifier is of interest. The symbol duration time for a bit rate of 100 GB/s in a 16-QAM modulation is about 40 ps. The measured PA group delay variation is about ±3 ps in the entire frequency band. Therefore the group delay variation is smaller than 10% of the symbol duration time, showing that the amplifier will not cause noticeable inter-symbol interference in communication systems.

For large-signal measurements, the amplifier can only be measured using two different high-power sources from VDI addressing 225-270 GHz (AMC 378) and 270-320 GHz (AMC 379), respectively. Both the input and output power of the power amplifier were measured using a PM4 power meter similar to the setup shown in [8]. Here, the losses of the waveguide bend and probe were deembedded using a 2nd-tier SOL calibration at the output. The presented compression behaviour and transducer power gain (Fig. 4) show the amplifier’s performance referred to the GSG pads. The measured transducer power gain is 0.8 dB smaller than the measured small-signal gain mostly due to the complex deembedding and low sensitivity of the PM4 for low input power levels. Similar to the small-signal measurements, the simulation shows higher gain, for small-signal measurements that difference was about 2 dB, which is here further increased due to the slightly lower measured transducer power gain. The measured amplifier shows an earlier compression resulting in an output referred $P_{1dB}$ compression point of 5.2 dBm and a maximum saturated output power of 6.4 dBm at 267 GHz. The model-to-hardware correlation is accurate for lower frequencies, while for higher frequencies this correlation deteriorates similar to the small-signal measurement and simulation differences.

Fig. 5 shows the saturated output power over frequency. The bandwidth is extended from 63 GHz to 89 GHz (226-315 GHz). The maximum output power of 6.7 dBm is reached at 272 GHz, here, large-signal gain could not be measured due to insufficient amplitude adjustment of the high power source. Without the balun losses, the amplifier is generates up to 8.1 dBm (Fig. 5). The extended bandwidth can be used for applications where linearity is not needed e.g. RADAR, material analysis or QPSK communication. Similar to the small-signal gain degradation, the output power degrades faster above 310 GHz than predicted by the simulation.

V. CONCLUSION

The presented amplifier achieves the highest small-signal 3-dB BW for silicon-based power amplifiers above 200 GHz while achieving a maximum $S_{21}$ of 17.9 dB (comp. Table I). The saturation behaviour of the amplifier extends the saturated power 3-dB BW to 89 GHz, thereby almost the entire J-Band is covered by the amplifier. The amplifier has the highest
This work was funded by the Deutsche Forschungsgesellschaft (DFG) within the projects DotSeven2IC (DFG PF 661/15-1) and project-ID 287022738-TRR 196; Project C04.

Fig. 5. Saturated output power of the amplifier measured with the two high power sources. For the measurement, both sources were set to maximum power at each frequency. A maximum output power of 6.7 dBm at 272 GHz was measured at the signal pad, the saturated output power 3-dB bandwidth was extended to 89 GHz, spanning from 226 GHz to 315 GHz. The maximum output power of 8.1 dBm without the balun losses at the output is shown as well.

generated output power for silicon-based power amplifiers in the J-Band. Without the balun, the amplifier is able to provide up to 8.1 dBm in an integrated system, while providing a small-signal peak $S_{21}$ of above 20 dB. The presented amplifier shows that advances in transistor technology allow silicon-based circuits to address new applications such as IEEE communication bands. The major challenge of broadband impedance transformation in power amplifiers was addressed by creating a transistor core layout allowing stable operation for both differential and common mode operation while keeping Q-factor deteriorations to a minimum. For matching engineers, creating coupled-line distributed transformers were developed to maximize the voltage swing at the output while realizing high impedance transformation ratios.

ACKNOWLEDGMENT

This work was funded by the Deutsche Forschungsgesellschaft (DFG) within the projects DotSeven2IC (DFG PF 661/15-1) and project-ID 287022738-TRR 196; Project C04.

### TABLE I

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>$f_{\text{max}}$ (GHz)</th>
<th>Operating 3-dB Frequency (GHz)</th>
<th>Small Signal 3-dB BW (GHz)</th>
<th>Peak $P_{\text{sat}}$ (dBm)</th>
<th>$O P_{\text{dB}}$ (dBm)</th>
<th>PAE (%)</th>
<th>Area (mm²)</th>
<th>$P_{\text{dc}}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>130-nm SiGe</td>
<td>550</td>
<td>228 - 256</td>
<td>28</td>
<td>10</td>
<td>5.5</td>
<td>1.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>[10]</td>
<td>130-nm SiGe</td>
<td>500</td>
<td>216 - 256</td>
<td>50</td>
<td>9</td>
<td>0</td>
<td>-2.5</td>
<td>0.5</td>
<td>0.33</td>
</tr>
<tr>
<td>[11]</td>
<td>130-nm SiGe</td>
<td>500</td>
<td>200 - 255</td>
<td>55</td>
<td>12.5</td>
<td>13.5</td>
<td>9</td>
<td>1</td>
<td>0.83</td>
</tr>
<tr>
<td>[12]</td>
<td>130-nm SiGe</td>
<td>500</td>
<td>247 - 238</td>
<td>11</td>
<td>21.5</td>
<td>0</td>
<td>-3.7</td>
<td>0.3</td>
<td>0.17</td>
</tr>
<tr>
<td>[13]</td>
<td>65-nm CMOS</td>
<td>400</td>
<td>195 - 209</td>
<td>14</td>
<td>19.5</td>
<td>9.4</td>
<td>6.3</td>
<td>1.03</td>
<td>0.392</td>
</tr>
<tr>
<td>This Work</td>
<td>130-nm SiGe</td>
<td>650</td>
<td>239 - 298</td>
<td>59</td>
<td>20.2***/17.9</td>
<td>8.1***/7.6/7.4***</td>
<td>5.2***</td>
<td>0.92***</td>
<td>0.26</td>
</tr>
</tbody>
</table>

*Uses power combiner. **Without Balun losses. ***Measured at 267 GHz.

### REFERENCES


