Enhanced data integrity of In-Ga-Zn-Oxide based Capacitor-less 2T memory for DRAM applications

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Abstract — IGZO (InGaZnO)-DRAM has been increasingly explored as an alternative to traditional DRAM due to its reduced transistor leakage (~10^-9A) and related minimal storage node capacitance in addition to ease of integration (entirely BEOL). The 2T0C IGZO-DRAM bit-cell configuration has additional benefits from a scaling point of view due to the potential for monolithic 3D stacking. We present a 2T0C IGZO based Capacitor-less memory that enhances the sensing margin and retention time for DRAM applications requiring higher data immaturity. In the proposed technique for increased data integrity, the Read Bit-Line (RBL) is precharged at Half-VDD, instead of Full-VDD, to utilize the rising edge of read word line (RWL) at the beginning of read. This increases the storage node potential of the bit-cell (due to coupling between RWL and the storage node) which is otherwise degraded at write termination due to coupling of write word line (WWL) and the storage node. From our simulation results, the proposed scheme (termed as HVPC-RBL) demonstrates stronger data integrity on data ‘1’ without the need for any additional cell capacitor. An additional benefit is the higher SN level (> 2X) resulting in higher sensing speed (10X) allowing reduced parasitic cell capacitance requirement ~1aF. This is 1000X less than the ~1fF parasitic cell capacitance required at the storage node for the conventional VDD-precharged RBL scheme (VPC-RBL).

Keywords— IGZO, Capacitor-less, 2T0C, gain-cell, noise immunity, parasitic cell capacitance, VPC-RBL, HVPC-RBL

I. INTRODUCTION

Currently, the application scope of 1T1C DRAM has increased from traditional regimes such as PC/Server/Mobile domain to include new ones like cloud/edge computing and artificial intelligence. However, below 20nm technology, it has become increasingly challenging for DRAM scaling to meet the demands put forward by these new application domains. These include the DRAM cell transistor’s ON-current requirements in order to ensure an operating speed faster than 10ns and the OFF-current target to assure long retention time s (e.g. > 64ms). Additionally, there are stringent requirements on cell capacitor (size and form factor) to maintain the memory cell efficiency and enough sensing margin (>100mV). In recent years, the In-Ga-Zn oxide-based field-effect transistor (IGZO-FET) has emerged as an alternative to the traditional DRAM transistor primarily due to its extremely low OFF-current (~3x10^-19A/μm) [9]. Thanks to this very low off current, a very small, the parasitic capacitance can be used to store the data and the storage capacitor becomes unnecessary. This very small storage capacitance, combined with the BEOL-friendly characteristics of IGZO-FETs enables further scaling of the DRAM bit-cell via the 2T0C IGZO-DRAM bit-cell configuration. As shown in Fig.1 (a), the 2T0C bit-cell is basically a 4-terminal structure governed by Write Word Line(WWL), Write Bit Line(WBL), Read Word Line(RWL) and Read Bit Line(RBL). During WRITE ‘0/1’, both WWL (above VDD) and WBL (VDD for ‘1’ or VSS for ‘0’) are triggered. The resulting charge that is stored at the internal Storage Node ‘SN’ can be observed by means of the voltage level developed on RBL during the READ operation. This is based on the VDD-Precharged RBL(VPC-RBL) scheme in the conventional scenario. The WWL can be used for minimizing the Write Transistor (WTR) off-current in its off-state. The absence of an external cell capacitor leads to a smaller bit-cell area but comes at the cost of increased sensitivity to noise and disturbance by parasitic coupling disturbance at the storage node. This enhances the risk on ‘Read Disturb’. The ‘capacitor-less’ feature in traditional, no IGZO, 2T0C bit cells also reduces the retention time (t_RET) of data ‘1’ due to the larger off-current originated from the NMOS of WTR. Thus, the storage cap node requirements of such 2T0C bit-cells typically leads to a larger parasitic capacitance (>1fF).

Fig. 1 (a) 2T0C memory bit cell configuration composed of two NMOS (b) The waveform of the VPC-RBL scheme resulting in reading ‘1’ failure due to lowered storage node level with smaller sensing margin (c) Simulation result of the SN degradation at storage node by WWL swing level.

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Fortunately, the retention time of IGZO-based 2T0C bit cells can also be managed with less dependency on the cell capacitance, thanks to the intrinsic super-low off-current features of IGZO-FET. The increased disturbance sensitivity that is intrinsic to 2T0C bit cells is highlighted in Fig.1 (b). We can see that after writing data ‘1’, i.e., storage node charged to V<sub>θp</sub>, the voltage on the capacitance is strongly deteriorated at the termination of write operation due to parasitic capacitance at the storage node. However, this leads the requirement of parasitic capacitance at the storage node is the corresponding timing operation. Based on these results, rules, the extraction of parasitic resistances and capacitances when V<sub>SL</sub> is determined as V=RBL’0’ – RBL’1’

Moreover, the voltage loss at the storage node is a consequence of IGZO-FET. The increased disturbance sensitivity deteriorated at the termination of write operation due to charged to V<sub>θp</sub> (negative voltage for body bias of cell transistor) to V<sub>PPW</sub> (positive voltage for WL boost) to bias our 2T0C cell. This gives a voltage range from -1.0V (V<sub>NN</sub>, the OFF-voltage bias @ WWL to regulate WTR off-current) to 2.0V (V<sub>PPW</sub>, as an ON-voltage bias @ WWL for the write operation) in our experiments. Secondly, the current drive of RTR is restrained to keep the footprint of the bit cell competitive with the conventional 1T1C DRAM device. Finally, the parasitic loading is derived from a 1Mb block size (1024 WLs x 1024 BLs) with a read/write latency below 10ns for DRAM-compatibility. From simulations, we identify 85nm as the required width (at minimal length) of the IGZO-FET to reach the target sensing margin (SM) of more than 0.2V. This is shown in Fig.2 (b). The layout rules are taken from a typical 28nm technology node. The storage node level is decided by WBL (i.e., written data) and the applied bias on the WWL (and thus WTR Gate; Fig. 1a). In case of write ‘1’, once the WWL level is applied above WBL+V<sub>θp</sub>, storage node level can be defined with WBL level. On the other hand, when the WWL is below than WBL+V<sub>θp</sub>, the SN is thus calculated as V<sub>PPW</sub> - V<sub>θp</sub>. This means that a lower V<sub>θp</sub> of WTR enables lower on-voltage bias at WWL during write ‘1’. A lower V<sub>θp</sub> is preferred for power saving. However, it also leads to higher off-current but this can be compensated by a applying V<sub>NN</sub> applied at WWL in standby. The value of V<sub>NN</sub> is determined from the target retention time.

II. IGZO-FET MODEL SETUP

In this work, the circuit-level simulations are based on a Verilog-A IGZO-FET compact model that is calibrated with silicon verified measurements. The critical parameters (such as Width, Length, V<sub>t</sub> and SS) are shown in Fig.1 (a). The resulting Id-V<sub>g</sub> characteristics of the IGZO-FETs is illustrated in Fig.2 (c). The assumptions and constraints for our IGZO based 2T0C bit cell are described below. Firstly, we apply the biasing conditions for the traditional 1T1C DRAM ranging from V<sub>θp</sub> (negative voltage for body bias of cell transistor) to V<sub>PPW</sub> (positive voltage for WL boost) to bias our 2T0C cell.

III. BIT CELL LAYOUT-BASED PARASITIC RESISTANCE AND CAPACITANCE EXTRACTION

Fig. 3 (a) shows the 2T0C bit cell layout with 28nm node rules. The bit cell area is 0.0875μm<sup>2</sup> based on I Contact-poly pitch (CPP). Since, the bit cell area of this layout is limited by Metal pitch (MP) rather than CPP, it is a more sustainable layout strategy for advanced nodes considering the more advantageous MP scaling trend compared to that of CPP beyond 10nm technology [2]. As shown in Fig.3 (b), parasitic resistance and capacitance of metal lines are extracted per cell. These values are then used for array-level simulations. Fig.3 (c, d) give the R and C values used. The coupling capacitances affect the storage node level depending on the operating mode. The total parasitic coupling capacitance at the storage node (C<sub>sn_para</sub>) is composed of 2 components: C<sub>pp</sub> and C<sub>pp</sub>. The interconnect layer between SN and the active region of WTR results in C<sub>p</sub>, whereas the gate capacitance of RTR results in C<sub>p1</sub>. Consequently, the total amount of C<sub>sn_para</sub> at the storage node can be influenced by the design rules for the inter-layer dimensions and gate capacitance of RTR. Hence, a larger size of RTR and increased inter-layer capacitance be used to increase C<sub>sn_para</sub>. As mentioned before, this total parasitic capacitance at the storage node affects the noise immunity of stored data and the retention time of 2T0C IGZO-memory. Therefore, the determination of C<sub>sn_para</sub> is quite crucial for the robust operation of the Capacitor-less 2T0C bit cell and can also impact the RTR sizing.

![Fig. 2 (a) The critical parameters in the behavior compact modeling of IGZO-FET](image-url)

**Fig. 2 (a)** The critical parameters in the behavior compact modeling of IGZO-FET (b) Simulation result of the develop of Read bit line (RBL) during the read operation by the Width of RTR at the scaled device in accordance with the target sensing margin higher than 0.2V (c) Ids-Vgs Characteristics of IGZO-FET modeled with Wd/Lg=85nm/27nm

Charge Injection (CI) and Clock Feedthrough (CF) [8] originating from coupling of the WWL to the storage node. Moreover, the voltage loss at the storage node is aggravated when V<sub>NN</sub> (Negative Voltage to turn off WTR) is applied at the WWL due to the resulting larger voltage swing (Fig.1 (c)). In traditional designs, this has been addressed by increasing the parasitic capacitance at the storage node. However, this leads to the higher area consumption and thus cell efficiency reduction. This on its turn negatively impacts to cost of the Memory. The objective of this study is to enhance the noise immunity of the storage node in an IGZO-FET based 2T0C bit cell (@ data ‘1’) via design innovation without resorting to increased parasitic cell capacitance. This paper is organized as follows. In Section II, we describe the IGZO-FET model. In Section III, based on a bit cell layout with 28nm technology rules, the extraction of parasitic resistances and capacitances for metal lines and the storage node is highlighted. Section IV presents the simulation results of the proposed schematic and the corresponding timing operation. Based on these results, the requirement of parasitic capacitance at the storage node is derived and design solutions to meet this requirement are discussed. Section V concludes the paper.
IV. RESULTS: SIMULATION AND TEST

Fig. 4 (a) shows the block diagram of the Half-precharged RBL(HVPC-RBL) scheme used in our simulations. It highlights the RBL precharge scheme (controlled by the RWL driver that is used to drive/precharge R(W)WL lines and the sense amplifier to detect written data). In this work, we consider a memory array size of 1Mbit, assuming 1024 cells each on both the W(R)WL and W(R)BL. For our simulations, the parasitics described in the previous section are considered. Fig. 4 (b) shows the waveform of the write operation followed by the read operation. Firstly, to write data ‘1’, WWL is driven to VDD. This voltage needs to be higher than VDD to transfer full-VDD to the storage node. However, while closing WTR, the SN level is degraded due to the capacitive coupling from SN and WWL. Meanwhile, RBL and RWL are precharged to Half-VDD and once the read command is activated, RBL enters into a floating state to detect the stored data at the SN. At the same time, RWL of the selected cell is driven by the decoding signal (from Half-VDD to a voltage higher than VDD, termed as VPPR).

As shown in Fig. 4(b), once the read command is initiated, the SN level is boosted by the coupling capacitance between RWL and SN(Cc3) (triggered by the rising edge of RWL from Half-VDD to VPPR). Accordingly, while reading data ‘1’, the enlarged VGS of RTR draws more read current leading to higher sensing speed as well as larger sensing margin under the same parasitic loadings. The optimal VPPR level is determined by the target for boosted VSN (with VPPR_MAX constrained by the device reliability of RTR). An additional benefit from the HVPC-RBL scheme is the relaxed on-current requirement of RTR due to boosted VSN. Since, the VSN level is not dominated by the write operation in the HVPC-RBL scheme, a low-Vt RTR is not necessary (compared to the VPC-RBL scheme) and a higher-Vt RTR leads to reduced off-current. Subsequently, this leads to an enlarged sensing margin for data ‘0’. Furthermore, it can also afford a single-Vt for both RTR and WTR in 2T0C bit cell configuration. On the other hand, while reading data ‘0’, the impact of the rising edge of RWL is diminished since the VSN level is also affected by the termination of write operation. The enablement of RWL can recover the degraded VSN level from below VSS.

Fig. 5(a) shows the simulation results comparing VSN dependence on Csn_para at the onset of reading data ‘1’ between the VPC-RBL scheme [8] and HVPC-RBL scheme. The VPC-RBL scheme can improve the SN level only by increasing Csn_para. Moreover, to achieve a VSN level above 0.8V for data ‘1’, nearly 1fF of Csn參 is required. The major advantage of the HVPC-RBL scheme is that we can maintain a constant and higher VSN level, independent from the Csn_para value. Therefore, with a smaller Csn_para value, the HVPC-RBL scheme ensures a higher VSN level than the VPC-RBL scheme. Fig. 5(b) shows the dependence of sensing speed on Csn_para for the two schemes. The HVPC-RBL scheme clearly shows better noise immunity at a smaller footprint. Our proposed HVPC-RBL scheme allows for a read access time <10ns even at a Csn_para of ~1fF. In Fig. 6, we compare the simulation results on the retention time for VPC-RBL and HVPC-RBL schemes. A retention time of 1s is achieved at 2.2V RWL biasing for the HVPC-RBL scheme (Fig. 6(a)). Furthermore, a higher RWL increases the retention time and exhibits a potentially ‘infinite retention time’. However, the maximum RWL level is limited by the
Fig. 5 (a) Dependence of storage node level on the parasitic cell capacitance between VPC-RBL and HVPC-RBL scheme at the onset of read operation. (b) Dependence of sensing speed on the parasitic cell capacitance between VPC-RBL scheme and HVPC-RBL scheme during read operation.

maximum voltage acceptable in the system compared to the conventional DRAM and by the device reliability. On the other hand, as shown in Fig. 6(b), the VPC-RBL scheme with the degraded SN level just after write results in a shorter retention time. Fig. 7 (a) shows the TEM image of the IGZO-based 2T0C test structure that was fabricated [9]. The timing from the read and write tests on the fabricated IGZO 2T0C bit-cell is shown in Fig. 7 (b)[9]. We can see that after charging the SN with 1V, the read operation is triggered by RWL activation. Subsequently, the SN level is boosted, so that read current from RWL can be measured. The details of the indirect assessment of VSN are reported in [9]. Fig. 7(c) indicates that the SN level of our proposed HVPC-RBL scheme is higher than the one of VPC-RBL scheme by ~1.4X. Table I compares this work to the state of the art, i.e., to IGZO-based 2T1C designs enabling long retention time at the cost of large (>1fF) storage node capacitance. In this work, we demonstrate that the 2T0C IGZO bit cell combined with the HVPC-RBL scheme only needs a Csn_para in the order of ~1aF. We thus, achieve a very cost-effective footprint combined with a longer retention time than classic DRAM.

V. CONCLUSION

In this paper a new IGZO based DRAM replacement is designed and demonstrated. It is based on a 2T0C bit cell with only parasitic storage capacitance. This cell is combined with a novel read write access scheme called HVPC-RBL to enhance noise immunity while maintaining sensing speed. The access scheme leverages on the read word line switching to enhance the SN charge at the end of the write operation.

Thus, we propose an attractive alternative to classic DRAM with comparable footprint but enhanced retention time.

Fig. 6 Comparison of retention time (a) VPC-RBL scheme to show the shorter retention time of data ‘1’ (b) HVPC-RBL scheme to recover the voltage loss of SN level supported by the rising of RWL in the beginning of read operation, respectively.

Table 1 Comparison with state-of-the-art works

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<td>Si-FET</td>
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<td>IGZO-FET</td>
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REFERENCES