An Optimized Low-Power Band-Tuning TX for Short-Range FMCW Radar in 22-nm FDSOI CMOS

Sammy Cerida Rengifo*, Francesco Chicco†, Erwan Le Roux† and Christian Enz*
Email: sammy.ceridarengifo@epfl.ch
*École Polytechnique Fédérale de Lausanne (EPFL) ICLAB, Neuchâtel, Switzerland
†Centre Suisse d’Électronique et de Microtechnique (CSEM) SA, Neuchâtel, Switzerland

Abstract—The paper presents a low-power transmitter (TX) as a part of a fully integrated 57-66 GHz FMCW radar system. The TX path includes a BPSK modulator and it is optimized for short-range operation with 0 dBm output power. A band-tuning technique is used for covering the 9 GHz band and it is tuned as the LO frequency is swept. The LO distribution is designed in a modular approach to be able to extend the number of TX paths for MIMO operation. Integrated in GF 22-nm FDSOI CMOS technology, each TX path is 570x100 µm² and consumes 17 mW.

Index Terms—FMCW, radar, mm-wave, low-power transmitter, power amplifier

I. INTRODUCTION

The millimeter-wave (mm-wave) frequency band around 60 GHz has been attracting interest for short-range devices (SRD) in the recent years thanks to the unlicensed ISM band from 57 to 66 GHz. The large spectrum available benefits short range sensing systems as frequency-modulated continuous wave (FMCW) radars, achieving a range resolution in the order of a few millimeters. Radars for automotive and industrial applications have been developing very rapidly focusing on high performance rather than low power consumption. Many of the current available radars in the market consume hundreds of milliwatts or even few Watts. However, those radars are not suitable for portable or Internet-of-Things (IoT) applications, where ultra low power consumption is required. Usually the most power-hungry block in this type of system is the transmitter (TX). Its power consumption becomes even more critical in the scenario of multiple-input and multiple-output (MIMO) radars where several TX channels are implemented to improve the angular resolution.

This work is part of a low-power fully integrated Radar-on-Chip (RoC), targeting the design optimization of a low-power TX for short-range radars. The paper is organized as follows. The TX architecture and design choices are described in Section II. Matching network optimization is explained in Section III. Measurement results are shown in Section IV, and finally conclusion is presented in Section V.

II. TX ARCHITECTURE

The TX block diagram, shown in Fig. 1, includes 2 TX channels. Each TX channel consists of three stages: 1. buffer, 2. modulator, and 3. power amplifier (PA). The purpose of the buffer is to increase isolation between the local oscillator (LO) and the subsequent stages, including additional TX channels. The modulator is used to generate signals that are orthogonal between each TX channel, it operates using BPSK implemented by chopping the differential branches. Finally, the PA is designed to deliver 0 dBm output power on a voltage supply of 0.8 V.

The TX signal path schematic is illustrated in Fig. 2. The amplification stages are based on the neutralized bootstrapped cascode amplifier (NBCA) topology [1]. Bootstrapping is implemented in the cascode transistor by increasing the capacitance $C_{DS,CASC}$. It can be seen, through Miller effect, as a negative capacitance in parallel with the common-source transistor, canceling out the parasitic capacitance $C_{DS,CS}$ [2]. This technique enhances the performance but creates a stronger feedback path from output to input leading to stability problems. Neutralization reduces the impact of the feedback path canceling out the capacitance $C_{GD,CS}$ and ensuring stability. In this type of PA the output nodes can theoretically reach a voltage swing of $2xV_{DD} = 1.6$ V. However, in an advanced technology node as 22-nm FDSOI, the safe operating voltage across drain and source needs to be as low as 0.9 V. Therefore, cascing improves reliability by preventing voltage stress.

The modulator was designed to operate with an IF in the order of a few MHz to benefit from the advantages of a low-IF architecture. Translating the beat frequency to a low IF is particularly interesting for SRD FMCW radars because otherwise it could fall in the range of hundreds of Hz and be degraded by the impact of DC offsets and flicker noise. The LO and buffer are supplied by two different low-dropout (LDO) regulators at 0.8 V to prevent any possible coupling. The modulator and PA are supplied by a third LDO to reduce any coupling coming from the modulated signal. The bias current in each stage of the TX is controlled by a 4-bit...
current DAC. Moreover, FDSOI technology provides flip-well transistors where the backgate can be used to apply forward body biasing. The transistor backgate is connected to their corresponding supply. This reduces the threshold voltage allowing higher drive and faster switching capabilities.

The two first stages are loaded by an interstage transformer and the PA is loaded by a balun matched to 50Ω Ground-Signal-Ground (GSG) pads. The center tap in each primary coil is connected to the corresponding supply voltage and the center tap in the secondary is used for biasing the common-source transistors of the next stage. Although the radar is required to operate across a very wide band, the FMCW signal is inherently narrow band. The 9 GHz bandwidth is covered using 3-bits thermometer capacitor banks to tune the resonance frequency of the inductive loads for each stage.

One of the main challenges in this design arises from the relatively high impedance required for the targeted low output power. Considering an ideal full voltage swing in the PA stage, the differential peak voltage is 0.8 V. The targeted output power is 0 dBm, which requires a differential impedance

\[ R_{PA} = \frac{V_{p}^{2}}{2P_{out}} = 320\Omega. \]  

(1)

The transistors in the PA stage must be sized for the calculated real impedance \( R_{PA} \), but there is a key parameter to take into account when designing for mm-wave in advanced technology node: the maximum frequency \( f_{\text{max}} \). This parameter is defined as the frequency at which the unilateral power gain is equal to unity, and in practice it is designed to be at least three times the operating frequency to guarantee enough power gain. However, in advanced nodes the gate resistance \( R_G \) can increase significantly depending on the number of fingers \( (N_f) \) that are chosen for a fixed total width, thus degrading \( f_{\text{max}} \). Fig. 3a shows simulations performed in a 10 µm wide NMOS transistor, finding an optimum minimum \( R_G \) for a finger width \( W_f \) of 0.5 µm. Moreover, \( f_{\text{max}} \) depends as well on the biasing current. In Fig. 3b a NMOS transistor designed with \( W_f = 0.5 \) µm and \( N_f = 20 \) is simulated for different current densities \( J_{DS} \). A value of 0.1 mA/µm is chosen as a good trade-off for low-power, obtaining a \( f_{\text{max}} = 208 \) GHz. Both common-source and cascode transistors in the PA were sized with a total width of 48 µm based on the chosen finger width and current density to achieve the required output impedance.

III. Matching Network Optimization

The balun model is shown in Fig. 4a. The matching approach is shown in Fig. 4b, this circuit is obtained by reflecting the impedances from the secondary to the primary. On the right side in Fig. 4b, the capacitor \( C_S \) is placed to resonate out the inductance \( L_S \). On the left side of the circuit a L-matching network is implemented to transform the load impedance \( R_L \) to match \( Z_{PA} \). The GSG structure is designed to match the load impedance \( R_L \) equal to 50 Ω. Furthermore, the goal is to make the secondary inductance \( L_S \) resonate without the need to add a functional capacitance. There is a parasitic capacitance already present in the GSG structure. This capacitance is equal to 44.6 fF and plays the role of \( C_S \). It is built using the transmission line (TL) connecting the balun with GSG pads. On the primary side, the L-matching network is designed for the same frequency as the secondary. Contrary to the transformer-based fourth order matching network [3] that provides a wider bandwidth, this design opts for a tuned transformer with higher quality factor to improve efficiency. The penalty of this design choice is a narrower band. Nevertheless, this is not a problem for FMCW radars since they do not need a fixed wide band.
The tuning capacitor banks are designed to switch in a 1 GHz network is 9 and the 3-dB bandwidth is approximately 6 GHz. At mm-wave, the calculated quality factor of the matching network depends on the parasitic capacitance in the primary and a smaller inductance ratio feasible to design at mm-wave. The calculated quality factor of the matching network is 9 and the 3-dB bandwidth is approximately 6 GHz. The tuning capacitor banks are designed to switch in 1 GHz steps and are implemented for each of the transformer in the TX path. The balun is designed as a co-planar structure, it uses the redistribution layer in order to minimize the parasitic capacitance from the bottom surface to the substrate but also to reduce the fringe capacitance compared to the case of using ultra thick layers. This type of structure with lower capacitive and magnetic coupling can achieve higher self-resonances frequency (SRF), maintaining a high quality factor and providing larger margin for parasitic capacitances.

The band-tuning TX operates synchronously with the FMCW sweep to cover the entire bandwidth, similarly to [4]. The channel TX2 is designed identically as TX1 from the transformer load of the buffer to the GSG pads. The LO distribution for the channel TX2 is taken from the output nodes of the TX1 buffer. This signal is connected to the input of the TX2 buffer which is loaded by a 400 μm-long TL connected to the first transformer in TX2. This long TL is very lossy because they are not designed in top metals, the latter are preferred for routing supplies all around the chip. These losses are compensated by the gain in the TX2 buffer, allowing to obtain very similar performances in both TX channels.

IV. MEASUREMENT RESULTS

The TX was fabricated in GF 22-nm FDSOI CMOS technology and was tested mounted on a board through on-chip probing using 200-μm pitch GSG probes (Picoprobes Model VMM65). The probe is connected through a coaxial 1 mm-cable to a coax-to-waveguide adapter (V281C). The operating frequency was measured by means of a Keysight PXA Signal Analyzer N9030A using a Waveguide Harmonic Mixer M1970V to extend the range from 50 to 75 GHz. Power measurements are conducted using an Agilent Power meter E4419B with a waveguide adapter for 50 to 75 GHz.

The chip microphotograph with two TX channels is shown in Fig. 6. The LO driving the TX channel is an on-chip 60 GHz Digital-Controlled Oscillator (DCO). The efficiency is defined as the TX output power divided by the power consumption of the entire TX channel (buffer+modulator+PA). Fig. 7 shows the output power and efficiency in channel TX1 for a fixed
TABLE I: Comparison with the state-of-the-art 60 GHz radar transmitters.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech</th>
<th>Freq (GHz)</th>
<th>VDD (V)</th>
<th>$P_{out}$ (dBm)</th>
<th>$P_{DC}$ (mW)</th>
<th>TX Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>65 nm Bulk CMOS</td>
<td>56.4-63.4</td>
<td>1.2</td>
<td>5</td>
<td>41</td>
<td>7.71</td>
</tr>
<tr>
<td>[6]</td>
<td>350 nm SiGe</td>
<td>57-64</td>
<td>3.3</td>
<td>4</td>
<td>990</td>
<td>5.61</td>
</tr>
<tr>
<td>[7]</td>
<td>130 nm SiGe</td>
<td>59.5-70.5</td>
<td>3.3</td>
<td>81</td>
<td>115</td>
<td>15.87 / 7.27c</td>
</tr>
<tr>
<td>[8]</td>
<td>28 nm Bulk CMOS</td>
<td>57-64</td>
<td>0.9</td>
<td>10</td>
<td>63 / 1375c</td>
<td>15.87 / 7.27c</td>
</tr>
<tr>
<td>[9]</td>
<td>28 nm Bulk CMOS</td>
<td>57-72</td>
<td>0.9</td>
<td>10</td>
<td>33.6 / 78.6c</td>
<td>29.76 / 12.72b</td>
</tr>
<tr>
<td>This Work</td>
<td>22 nm FDSOI CMOS</td>
<td>57-66</td>
<td>0.8</td>
<td>1</td>
<td>13.5 / 17.6</td>
<td>9.33 / 7.15c</td>
</tr>
</tbody>
</table>

* Entire radar power consumption (VCO+2TX+4RX).  
* LO distribution (buffers) not included.  
* Estimated including LO distribution.

Fig. 7: TX1 Measurements versus power consumption at 62 GHz: (a) Output Power (b) Efficiency.

Fig. 8: TX1 Measurements versus frequency: (a) Output Power (b) Efficiency.

Fig. 9: TX2 Measurements versus frequency: (a) Output Power (b) Efficiency.

frequency of 62 GHz as the biasing current DAC increases the power consumption of the TX. The saturated output power is 1 dBm consuming as low as 17 mW for maximum efficiency.

Fig. 8 shows the saturated output power and efficiency versus the frequency for the multiple tuning bands. The output power varies from -5 to 1 dBm across the 9 GHz bandwidth. In Fig. 9, the measurements of channel TX2 show a slightly narrower band compared to TX1. The parasitic capacitance in the TL distributing the LO to TX2 were underestimated. Thus the band-tuning step is smaller than the expected 1 GHz and the saturated output power is lower at the edges of the operating band. The DC power consumption in both TX channels is the same. The buffer, modulator, and PA consume 3 mW, 4.3 mW, and 9.8 mW respectively.

The TX performance is compared to state-of-the-art radars in Table I. Most of the work in literature target applications that require higher output power, which makes this work one of the first optimized TX for such a low output power. Some of the work report the TX power consumption and efficiency without taking into account the LO distribution. The buffers needed to distribute the LO signal at mm-wave can consume as much as the TX channel. The power consumption of LO buffers is estimated in [8] and [9] for allowing a fair comparison. The TX efficiency is comparable to other state-of-the-art FMCW TX in the 60 GHz band. Moreover, this paper reports the lowest power consumption for FMCW TX, while delivering enough output power to operate in a short range up to a few meters [6].

V. CONCLUSION

A low-power band-tuning 60 GHz TX has been implemented in GF 22-nm FDSOI CMOS technology. Several mm-wave design techniques and a matching network optimization have been used in order to achieve a good performance for low-power FMCW radars. The tuned matching network for each TX stage allows to benefit from a higher quality factor in a narrower band and synchronously sweep LO and TX bands to cover the entire 9 GHz band. Each TX channel consumes only 17 mW and outputs a saturated power of 1 dBm.

REFERENCES