Experimental Assessment of Variability in Junctionless Nanowire nMOS Transistors

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I. INTRODUCTION

Junctionless (JL) nanowire transistors have been proposed to circumvent the challenge of fabricating ultra-sharp junctions in extremely scaled inversion mode (IM) MOS transistors [1, 2, 3]. The absence of junctions makes the process fabrication simpler and the good immunity to short-channel effects contributes to make junctionless nanowire transistors a promising candidate to continue the downscaling of MOS transistors. However, an important characteristic that must be considered in the scaling of a device is the variability of its electrical parameters [4, 5].

Several works based on TCAD and Monte Carlo simulations show that the random doping fluctuation (RDF) appears to be a major source of variability in junctionless nanowire transistors, due to the ultra-high doping in the channel associated to the reduced silicon volume [6 - 9]. Although these and many other works report simulations and modeling of variability in JL nanowire transistors, to the best of authors’ knowledge, only one recent work available in the literature presents experimental study of variability in JL devices [10]. Therefore, this work presents experimental assessment of junctionless nanowire variability, extending and complementing the achievements of [10] to different bias conditions and channel lengths. Die-to-die variability of threshold voltage, drain-induced barrier lowering, drain current and transconductance is shown for junctionless nanowire transistors. Also, a comparison with inversion mode nanowire transistors fabricated in the same technology is presented.

II. DEVICES AND MEASUREMENTS DETAILS

N-channel silicon nanowires have been processed at CEA-Leti, France, from 300 nm <100> SOI wafers featuring buried oxide layer with a thickness of 145 nm [10]. Both junctionless (JL) and inversion mode (IM) transistors present Ω-gate shape, as schematically represented in Fig. 1, which presents the cross-section and top view of a fin, whose height is 10 nm. The gate stack is composed of 2.3 nm CVD HfSiON / 5nm ALD TiN and 50 nm polysilicon. The resultant effective oxide thickness (EOT) is around 1.2 nm. Devices with a channel length (L) of 40 nm and 100 nm, 10 parallel channels with effective fin width (Wfin) of 12 nm, 17 nm, 22 nm, and 42 nm were measured. Drain current (Id) curves as a function of gate voltage (Vg) at drain-to-source voltage drop (VDS) of 40 mV and 800 mV have been obtained using a semiconductor parameter analyzer Keysight B1500. In-wafer variability is studied by measuring the same device on different dies randomly chosen across the wafer. The number of measured devices is 25 for JL and 22 for IM devices.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Threshold voltage variability

The threshold voltage (VT) has been extracted from drain current curves as a function of gate voltage, with 1 mV-step for accuracy, at VDS = 40 mV, using the double derivative method [11]. By adopting the total width as Wt = N×(Wfin + 2×Hfin), N is the number of parallel channels, Pelgrom plot [12] of σVT of junctionless and inversion mode nanowires has been obtained and is presented in Fig. 2. It can be seen that the matching coefficient (AVT), given by the slope of the linear regression is worst (higher) for JL devices than IM. The values found in this work are higher than those presented in [10], which presents local variability.

Threshold voltage variation is a result of random mismatch of technological parameters such as doping concentration, silicon film, and gate oxide thickness [13]. In nanowire MOS transistors, the gate workfunction and doping concentration are the main sources of threshold mismatching.
In agreement with the experimental data of [10], the variability is larger in JL nanowires than in inversion-mode ones, which is related to random doping fluctuation, as predicted by TCAD and Monte Carlo simulations [6 - 9]. However, the obtained standard deviation of JL transistors is smaller than the values reported by atomistic simulation and models in [8], which is around 50 mV for L = 100 nm, and 70 mV for L = 50 nm for cylindrical nanowires with a radius of 10 nm, whose dimensions are close to the nanowire of WFIN = 12 nm. Also, differently from the results reported in [14] for IM undoped FinFETs, the scaling of both WFIN and L worsens the threshold voltage variability.

The threshold voltage with devices biased in saturation has been also extracted using the constant current method [11]. In order to account for the different mobility and dimensions of devices, the current level for each group of devices with the same dimensions has been defined as the increase of matching coefficient (A\text{VT}) for IM undoped FinFETs, the scaling of both WFIN and L worsens the threshold voltage variability.

![Pelgrom plot of σVT for Junctionless and Inversion Mode nanowire nFETs biased at VDS = 40 mV and 800 mV.](image1.jpg)

Fig. 2. Pelgrom plot of σVT for Junctionless and Inversion Mode nanowire nFETs biased at VDS = 40 mV and 800 mV.

The remarkable mean DIBL of 40 mV/V for L = 40 nm JL nanowire with WFIN = 12 nm confirms the excellent electrostatic control provided by this device architecture.

The standard deviation of DIBL as a function of fin width for junctionless nanowires.

B. Drain current variability

![DIBL measured for the JL nanowires of different channel lengths and fin widths, at VDS = 40 mV and 800 mV.](image2.jpg)

Fig. 3. Drain-Induced Barrier Lowering measured for the JL nanowires of different channel lengths and fin widths, at VDS = 40 mV and 800 mV.

For the devices biased in this condition, the relative deviation of drain current tends to a constant value. At similar VGST = 500 mV, the σI\text{DS}/I\text{DS,mean} of the narrow and short device degrades from 5% to 8.5% when the nanowire changes from IM to JL mode.
The maximum transconductance ($g_{m,max}$) for devices biased at low $V_{DS}$ (40 mV) has been extracted from the derivative of drain current curves. It can be approximated that the maximum transconductance depends on the mobility and the series resistance, which are components that can affect the current variability. The obtained relative deviation ($\sigma_{g_{m,max}}/g_{m,max,mean}$) is presented in Fig. 6, in a Pelgrom plot, for junctionless and inversion mode devices. One can note that the relative deviation of the transconductance coincides with the plateau of the current deviation, indicating that the series resistance and mobility are the components dominating the mismatching. According to [10], the series resistance relative variation is similar in JL and IM mode devices. Therefore, since mobility is doping-dependent, RDF impacting junctionless nanowires are likely to be responsible for the higher current variability for a given voltage bias, even when $V_T$ variation is neglected in the current deviation analysis. For the presented results, the matching coefficient for the maximum transconductance in junctionless nanowire transistors is almost twice the coefficient for inversion mode transistors.

In order to account for the different current levels in JL and IM devices, the relative current deviation is presented as a function of the mean current for JL and IM devices with $L = 40$ nm and 100 nm, in Fig. 7(A) and (B), respectively. As can be seen, for long-channel devices, at the same current level, junctionless nanowire transistors present larger variability than inversion mode ones with the same $W_{FIN}$. As devices are shortened, the drain current variability increases, both for JL and IM nanowires. However, due to the good SCE immunity, associated with the longer effective channel length at smaller gate voltages [16], i.e. smaller $I_{DS,mean}$, JL devices increase of $I_{DS}$ variability is less pronounced than for IM ones. Therefore, for devices with $L = 40$ nm, junctionless nanowire transistors present less variability than IM counterpart. At $I_{DS,mean} = 5 \mu m$, the relative current deviation is 67% higher in the IM device than JL, both with $W_{FIN} = 12$ nm. This result is in accordance with those presented in [10] for 18 nm-long nanowires.

Aiming at evaluating the variability impact on the current of devices in a practical circuit operation condition, the drain current deviation has been obtained at $V_{DS} = 800$ mV. The results are presented in Fig. 8 for JL and IM nanowires with $L = 100$ nm, obtained at the same $V_{GS}$ (top x-axis) and $V_{GS} - V_{T}$ (bottom x-axis). It has been observed that the current deviation is slightly affected by the drain voltage increase when comparing the results presented in Fig. 5.
Fig. 9(A) shows the drain current relative deviation (\(\sigma_{\text{IDS}}/\text{IDS}_{\text{mean}}\)) devices as a function of \((W_T \times L)^{1/2}\) for devices with different channel lengths and fin widths biased at \(V_{DS} = 800\,\text{mV}\), which would be a common operation point in digital circuits. The matching coefficient \(A_{\text{IDS}}\) is slightly higher for junctionless devices \((1.143 \times 10^{-2}\,\mu\text{m})\) in comparison to inversion mode \((8.7 \times 10^{-3}\,\mu\text{m})\). However, comparing the matching coefficient obtained for \(g_{\text{ln,\text{max}}}\) (which is approximately the same as the current at low drain bias) one can note a small degradation with \(V_{DS}\) increase in JL nanowires, while a larger increase is observed for inversion mode devices. It might indicate that in saturation at high gate bias, the mobility variation due to the perpendicular field can be larger in IM mode than in JL devices.

Besides to its attractive operation in digital circuits, JL nanowires demonstrate improved analog figures-of-merit than IM ones [17]. Analog circuits are often biased at low gate overdrive voltage to ensure good performance and bias swing. Therefore, to evaluate the variability impact in this kind of circuits, Fig. 9 presents the Pelgrom plot of drain current relative deviation \((\sigma_{\text{IDS}}/\text{IDS}_{\text{mean}}))\) for all devices biased at \(V_{DS} = 800\,\text{mV}\) and \(V_{GS} - V_{T}\) = 200 mV. The matching coefficients are smaller than at higher gate bias (Fig. 8). However, the reduction of the matching coefficient is more pronounced in IM nanowires than for JL ones which is correlated with the worst \(V_T\) matching in the later.

IV. CONCLUSIONS

This paper presented experimental results of variability in JL nanowire transistors. It has been shown that threshold voltage variability can be smaller than that predicted by TCAD and atomistic simulations reported in the literature. Although threshold voltage variability of JL nanowires can be higher than in IM ones, it does not significantly affect drain induced barrier lowering deviation, which has shown to be smaller than 8 mV/V in the shortest and narrowest device, indicating that it has a negligible effect when devices are biased in saturation. The ratio between the deviation of drain current of JL and IM devices has shown to reduce when devices operate at high drain and gate voltages, reducing from 3 to 1.3 times when increasing \(V_{DS}\) from 40 mV to 800 mV. Is has been shown that as the channel length is reduced, the current variability in JL becomes smaller than in IM mode devices with same dimensions at the same current level, owing to its immunity to short-channel effects.

REFERENCES